

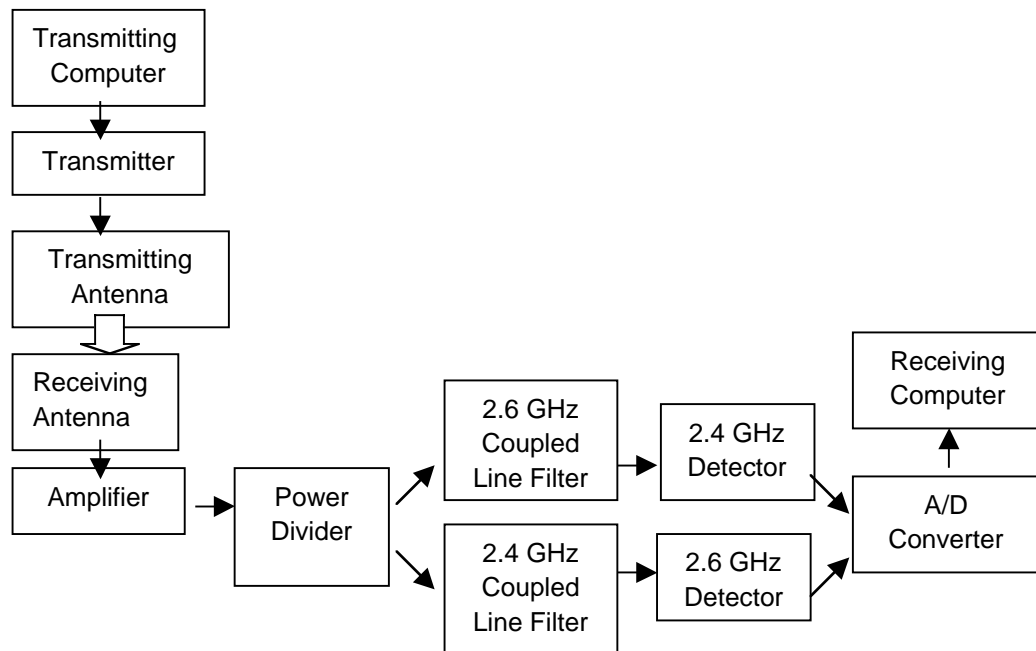


## Technical Report: Overview of a Wireless Local Area Network (WLAN)

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As wireless applications are becoming more and more predominant today, it is interesting to become familiar with some of the aspects of wireless design that must be faced and overcome. The objective of this Senior Project is to build a wireless local area network that operates in the microwave frequency range. A majority of the components in the design are designed using Libra software since they are microstrip circuits. An explanation of each of the components in the design is included in this Technical Report.

Figure 1 shows a system level diagram of the wireless local area network. The circuit consists of two parts, a transmitter (the three blocks on the left of the figure) and a receiver (the remainder of the blocks). The transmitter takes binary data from the transmitting computer through the serial port and uses frequency shift keying to produce two transmitted frequencies. A binary 1 is represented by a frequency of 2.4 while a binary 0 is represented by a frequency of 2.6 GHz. These frequencies are transmitted through an antenna. An antenna at the receiver picks up the transmitted signal. The signal instead of propagating through the air is present on a microstrip transmission line and is amplified using a high frequency amplifier.



**Figure 1. System Level Diagram: A Wireless Local Area Network**



then used to convert the RF signal to a DC voltage when a signal is present on the line. Each detector circuit is matched to reduce the power of the reflections at the frequency that is allowed to pass through the bandpass filter. A comparator distinguishes the predominant signal at the output of the detector circuits and is used as an A/D converter. The digital signal output from the comparator is then input to the receiving computer through the serial port where a software interface displays the received signal on the terminal. The overall operation of the circuit takes the characters typed on the transmitting computer and displays them on the monitor of the receiving computer.

### **The Transmitter**

The transmitter for the project makes use of the Agilent ESG-3000A Signal Generator. Characters are output through the serial port of the transmitting computer. In this case they are digital 1's and 0's. A high-speed op amp is used as a comparator to convert the voltages from the computer (-12 V or 12 V) to a voltage on the rail of the op amp, which will be used to select either 2.4 or 2.6 GHz. The expected offset frequency is 2.5 GHz when linear frequency modulation occurs. This signal generator was found to be nonlinear in this range which may be due to the fact that its highest frequency is 3 GHz. An offset frequency of 2.57 GHz, was found to allow a frequency swing from 2.4 to 2.6 GHz. The voltage necessary to produce 2.4 GHz is -2.91 V and that necessary for 2.6 GHz is 2.11 V. The non-inverting input of the op amp was grounded, and the inverting input was connected to the transmit pin (pin 3) of the DB-9 serial port of the transmitting computer. The rail voltages were set to produce the output voltages as specified above. The chassis ground (pin 5) of the serial port was also connected to ground along with the voltage supply ground and the ground lead from the external input of the signal generator. The op amp controller for the signal generator was tested and found to provide the proper frequencies for transmission when bits were transmitted through the serial port.

The interfacing software for serial communications was obtained from a Computer Engineering student who wrote parts of it as an assignment in Dr. Abbot's ECE 5780 class. The program is designed to both transmit and receive. In this case it is used for uni-directional transmission and reception. The software allows for more complex bi-directional circuits in the future.

### **Antennas**

Ideally, the antennas used for this project should be directional with good matching networks that provide a low standing wave ratio (SWR). Antennas that have some of these qualities can be purchased, but a more conducive method for learning is to build a set of antennas. A simple dipole antenna can have a good SWR at both of the frequencies that are used in the circuit. The only problem with it is that it is not directional. For this project a set of antennas is used. One is a microstrip fed monopole above a ground plane and the other is a biconical antenna.

The monopole antenna is built by attaching a length of non-insulated copper wire to a microstrip line with a ground plane. The length of the wire is approximately 3 cm. The response can be tested using the Agilent 8510 Network Analyzer. The antenna response can be modified by shortening the wire or by adding open-circuit stubs using copper tape to the microstrip line to help match the antenna at the input. In the case of the dipole antenna, two small pieces of tape caused the standing wave ratio to be reduced to less than 1.5 at both frequencies of interest.

The biconical antenna was built using copper sheeting and the base of an aluminum can. After matching the antenna, a standing wave ratio of about 1.9 at both frequencies was attained. By designing another dipole antenna, a more efficient link could likely be attained. The advantage of a biconical antenna is that it is not strictly a horizontal receiving antenna. It could be used in a multi-floor network when sufficient power is available to make it feasible. For the purposes of this project, these antennas are adequate.

One antenna is attached to the transmitter, and the other is connected on the front end of the receiver. At the present, the available power is a problem. More amplification would be desired either before



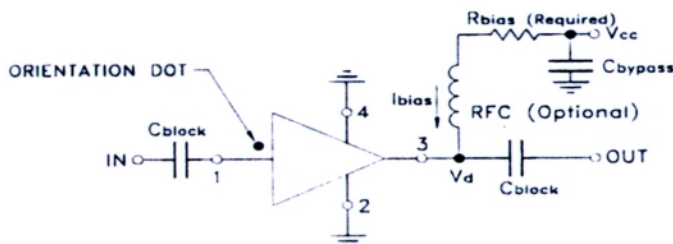
transmission occurs or after reception of the signal. The antennas and connectors are the weak link in the circuit. In a future project, more time could be spent in designing a well-matched, directional antenna. Some possibilities for better antennas are a dipole with a corner reflector, a patch Yagi Uda, or a patch log periodic antenna.

### Amplifier Circuit

Amplification is necessary in a wireless network. The reduction in the signal due to losses during transmission, reception, and power dissipation in circuit components must be compensated by using a device to provide sufficient gain for the receiver circuit. Some real world issues when choosing an amplifier are its cost, size, and gain. The gain of the amplifier element correlates with the range that can be obtained by the link.

For the wireless LAN circuit, the ERA-3SM amplifier from MiniCircuits is used. It provides about 15 dBm gain at the two operating frequencies.

To provide for correct functionality, the choice of circuit components is critical. A schematic illustrating the necessary components is shown in Figure 2. A proper bias current is achieved by placing a resistor on the DC bias branch of the circuit. The amplifier also requires DC blocking capacitors at its input and



**Figure 2. Amplifier Schematic from MiniCircuits RF Designer's Handbook 1998**

output to allow only the high frequency signals to enter the passive circuitry.

Surface mount components are used to reduce the inductive effects produced by long leads in high frequency applications.

DC blocking capacitors are necessary on the input and output of the amplifier to block DC voltages and allow the RF signal to pass. The data sheets specify that the capacitors "should have a low effective series resistance (ESR) and should be free of parasitic (parallel) resonance up to the highest operating frequency." The value of

the capacitance is not specified in this case, but 100 pF seems to be a very common value for this type of application. With some searching, capacitors can be found that have a low ESR and a parallel resonance that is above 2.6 GHz.

Using a 12 VDC supply, a bias current of 35 mA is desired for proper operation. For this current, the DC bias branch should contain a resistor with a value of 243 ohms that can dissipate at least 300 mW of power. The resistor used in this circuit has a value of 240 ohms and power dissipation of 350 mW.

To improve the gain of the amplifier, an inductor can be used in the bias branch to reduce the amount of RF power that is lost in the branch. The value of the inductor is chosen to be larger than ten times the load impedance (in this case, the load impedance is the characteristic impedance,  $Z_0 = 50$  ohms). The inductor must also be "free from parasitic (series) resonance up to the highest operating frequency." An inductor with a value of 47 nH is used in the circuit. The use of a bypass capacitor is also desirable in the bias branch to approximate a steady input current. The value of the capacitor is 100 pF. The layout of the



amplifier circuit with component values as labels is shown in Figure 3.

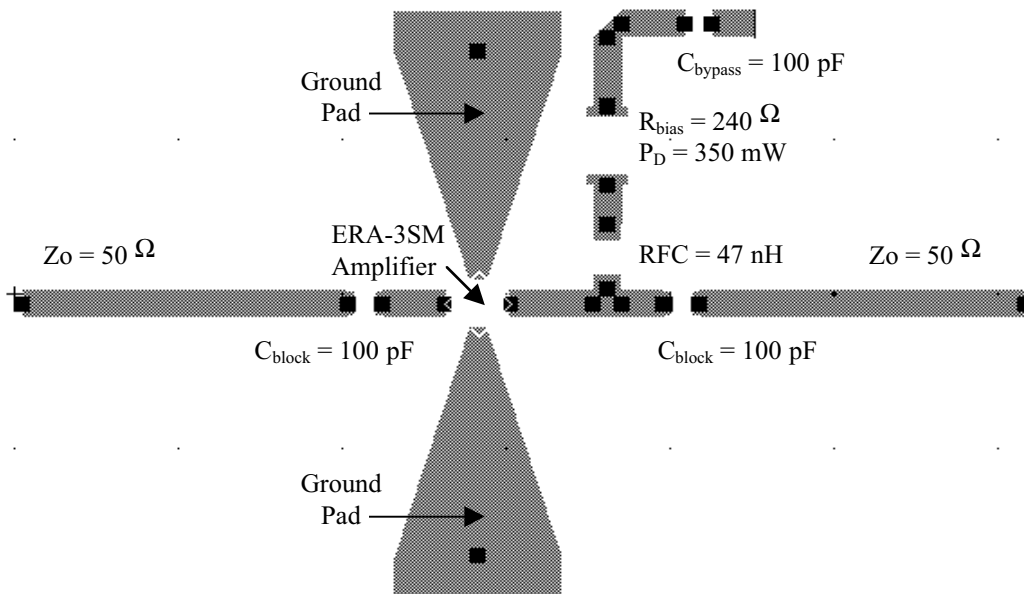


Figure 3. Amplifier Layout

An important issue when using RF amplifiers is the issue of grounding. The grounding for the amplifier must be very good. An example of the dimensions of ground pads that are sufficient for proper operation of the amplifier are illustrated in Figure 3. Holes are drilled through the pads, and ground pins are soldered from the pads to the ground plane underneath. It is very important to ensure that ground pins are placed near to the grounding pins of the amplifier to reduce the high-frequency effects.

When preparing the layout for the circuit, spacing for the amplifier and other components must be allotted to allow room for soldering the components. This is done in the Libra simulation software. The artwork for a transistor can be used to prepare space for the amplifier since there is no amplifier layout in the libraries. Space for other components is allotted by using lumped elements with artwork and pads. The case sizes for each of the components can be found on their respective data sheets. Some unit conversions may be necessary depending on the values that are specified. When the circuit design is complete in the Schematic window, the circuit is synchronized and can be viewed in the Layout window where the sizes can be verified, and the overall circuit size is noted. The circuit is exported in HPGL format, prepared for milling using CircuitCam software, milled on the proper substrate, and soldered preferably using the surface mount equipment in the senior design room.

The circuit can be tested in two ways. The first method is to use the Agilent 8510 Network Analyzer to view the overall performance of the amplifier. The amplifier gain can be seen over the frequency range of interest after calibrating the Network Analyzer. Another method is to test the circuit using the Agilent ESG-3000A Signal Generator on the input of the amplifier and the Agilent 8594E Spectrum Analyzer on the output to see the gain at discrete frequencies. The same circuit holder that is used for TRL measurements on the network analyzer is used to connect the microstrip circuit to the coaxial lines for the input and the output of the circuit. For amplifiers with a gain higher than 15 dBm, the network analyzer does not display the correct information for the gain, and the signal generator and spectrum analyzer must be used. This is especially true when multiple amplifiers are cascaded to produce higher gain circuits.

### Power Splitter

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The power splitter (3-dB coupler) is the next sequential component in the circuit. The input of the circuit needs to be matched to the characteristic impedance of 50 ohms. Equal power is desired on both



branches of the output circuit. As an optional constraint, each branch of the circuit can be tuned to the frequency that will eventually be detected on that branch, 2.4 and 2.6 GHz, by using quarter wave transformers.

A schematic of the power divider is shown in Figure 4. The input line of the power divider is 50 ohms. This value is obtained by milling a line with the proper width as dictated by using Linecalc in the Libra software package. For effective matching, the equivalent impedance of the two parallel lines of the output should

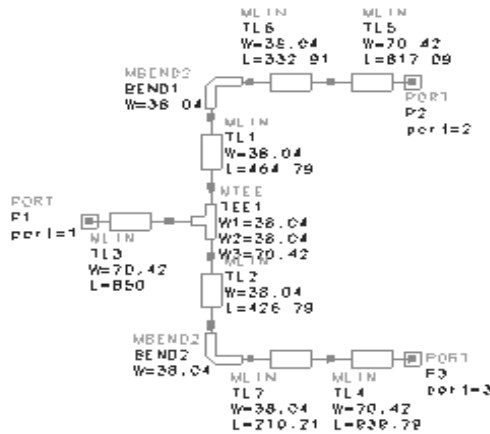


Figure 4. Power Divider Schematic

also be 50 ohms. The parallel combination of two 100 ohm lines will produce the proper matching and power division. Since the eventual output of the power splitter will also need to be matched to 50 ohms, a logical choice is the use of quarter wave transformers. The length of the 100 ohm line can be zero since a quarter wave transformer can be placed on each branch immediately after the input line is split. The impedance for the quarter wave transformer is found by taking the square root of the 100 ohm impedance times the 50 ohm impedance producing 70.71 ohms. The length and width of the microstrip lines is found by using Linecalc in Libra with an electrical length of 90 degrees (one quarter wavelength) at each respective frequency and a characteristic impedance of 70.71 ohms. (See Microwave Engineering by David Pozar pp. 359-362).

The circuit can be simulated using the test bench in Libra. A frequency sweep is desired from about 2-3 GHz. The parameters of interest are S11, S21, and S31. The simulation for the reflection coefficient, S11, is shown in Figure 5. This parameter is a measure of how well the input of the power splitter is matched. Plots of the two transmission coefficients, S21 and S31, are shown in Figure 6. The responses can be tuned by shortening or lengthening the quarter wave sections until a low (less than or equal to -20 dB) reflection coefficient is attained and transmission coefficients with values near -3 dB are attained. The schematic is then synchronized, exported, and

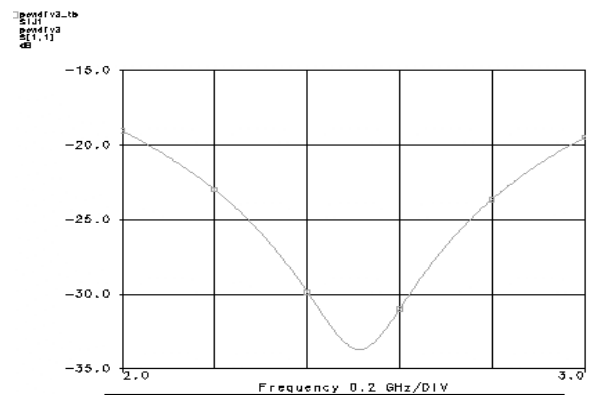


Figure 5. Power Divider Simulation for S11

milled. The layout for the power divider is shown in Figure 7.

Testing is performed on the circuit using the Agilent 8510 Network Analyzer. After calibrating the ports using the TRL calibration, the parameters for S11 and S21 can be measured. When this measurement is performed, the third port should have a matching load placed on it so that there will not be any reflections due to an unmatched termination. The circuit can then be rotated 180 degrees, and the value for S31 can be attained by placing the matched load on the port that is not connected to the network analyzer.

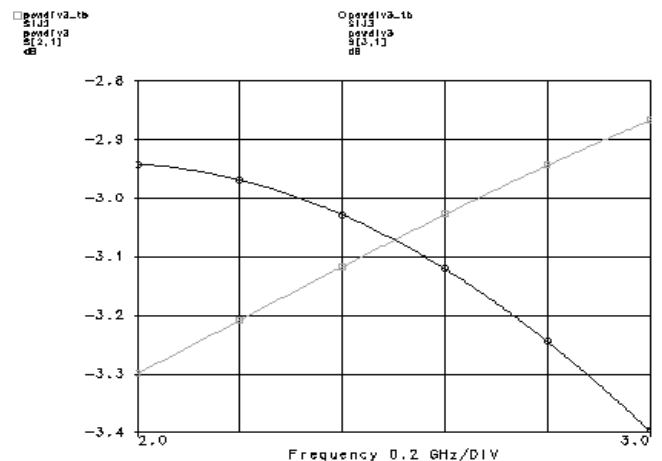


Figure 6. Power Divider Simulation for S21 and S31

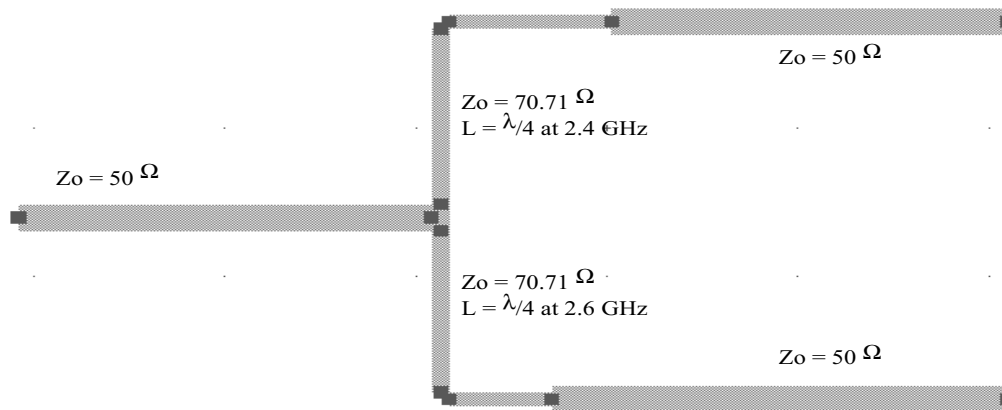


Figure 7. Power Divider Layout

### Coupled Line Filters

To distinguish which signal is present on a line of the circuit, bandpass filters are used. A pass-band of 100 MHz is desirable with an insertion loss that is as low as possible. The falloff in the stop bands should be steep with values at the opposite frequency of at least  $-30$  dB. A ripple of 0.5 dB is sufficient for the design. The filter should also be matched to the characteristic impedance of 50 ohms.

Bandpass filters can be designed using coupled lines in microstrip. When designing the filters, normalized frequencies and impedances are used. In Table 1, the parameters for fourth order coupled line filters that meet the specifications for this project are shown. These values are used in the Libra software package to find the lengths, widths, and separations for each of the respective coupled line sections. This process is performed at both 2.4 and 2.6 GHz to produce the microstrip implementations of the circuits as shown in Figure 8. Each filter section is one quarter wavelength long (*Microwave Engineering* by David Pozar pp. 475-485).

TABLE 1. COUPLED LINE FILTER PARAMETERS				
Delta = 0.5	$g_n$	$Z_o J_n$	$Z_{oe}$	$Z_{oo}$
S1	1.6703	0.216844	63.19328	41.50886
S2	1.1926	0.055647	52.93719	47.37246
S3	2.3661	0.046755	52.44704	47.77156
S4	0.8419	0.055647	52.93719	47.37247
S5	1.9841	0.216837	63.19275	41.50907

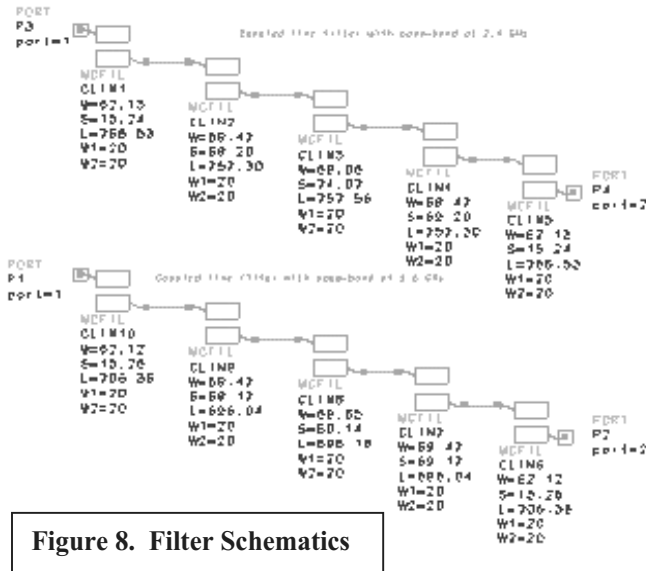


Figure 8. Filter Schematics

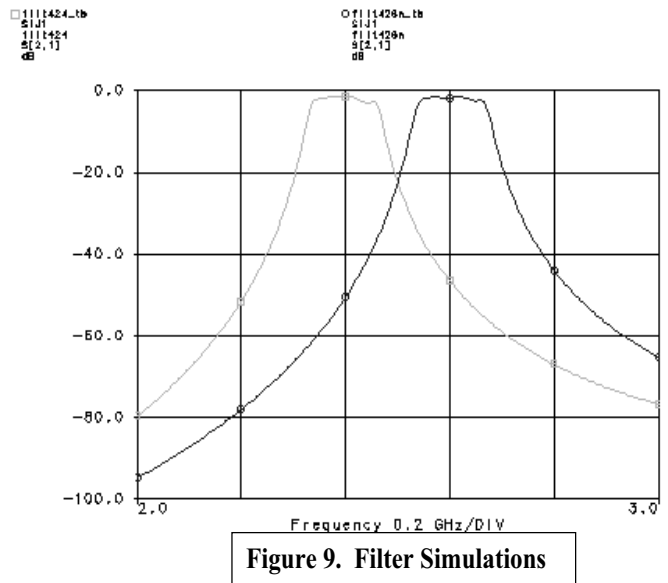


Figure 9. Filter Simulations

The simulation of each circuit is performed using the test bench in Libra. A plot of the simulations for both the 2.4 and 2.6 GHz filters is shown in Figure 9. The frequency sweep is from 2-3 GHz and the parameter of interest is the transmission coefficient,  $S_{21}$ , from the input port to the output port for each filter. As can be seen in the plot, the filters have smooth responses and steep falloffs outside the pass-band. When the plots appear as they should (pass bands for 2.4 and 2.6 GHz respectively), the schematics are ready to be synchronized, exported, and milled. The layout of a coupled line filter is shown in Figure 10.

The circuits are tested using the circuit holder on the Agilent 8510 Network Analyzer. The TRL calibration is performed. Once again, the  $S_{21}$  parameter should be measured. The response for each filter should correspond closely with the response produced in Libra.

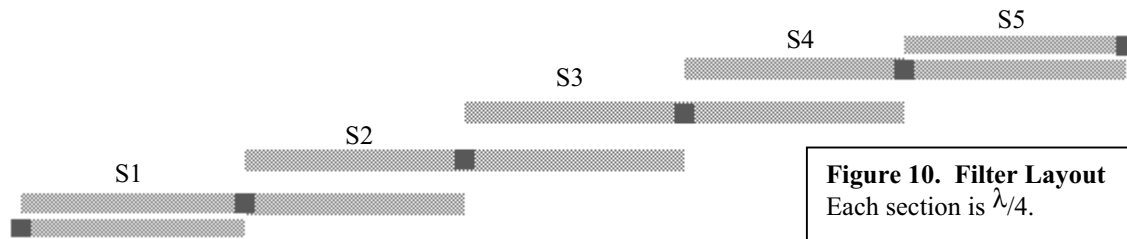


Figure 10. Filter Layout  
Each section is  $\lambda/4$ .

The signal generator and spectrum analyzer can also be used to test the response of the filters. The signal generator should be connected to one side of the circuit via the circuit holder, and the spectrum analyzer should be connected to the other side of the circuit. In the case of the filter, the circuit is symmetric. It does not matter which side is used for input and which is used for output. The spectrum analyzer will show what power is output when a constant power is input from the signal generator. The frequency range can be swept, and the response should correspond to the one obtained from the network analyzer.



### Detector Circuit

The goal of the detector circuit is to convert a high frequency signal into a DC voltage. In this case, a diode rectifier and integrating capacitor are used to meet this goal. An effective matching circuit is needed to prevent reflections and maximize the power input to the diode detector circuit. Detector circuits with matching networks are shown in Figure 11.

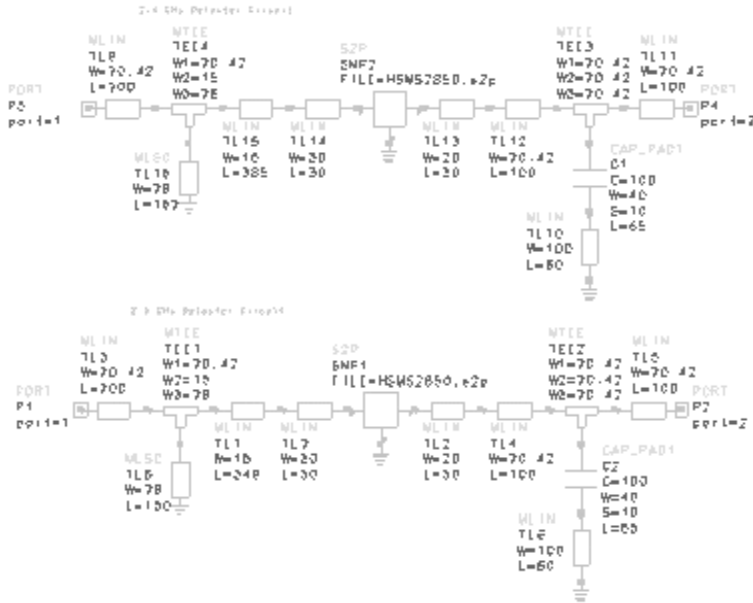


Figure 11. Detector Schematics

Since diodes are non-linear devices, proper matching is a formidable task. This is due to the fact that the input impedance of the diode is very close to the outside of the Smith Chart. The most effective way of finding the load impedance of the detector circuit is to build a circuit with a known length of line on the front, measure its input impedance with the network analyzer, and calculate the load impedance at the diode by rotating the input impedance on the Smith Chart by the known length of the line. Matlab code can then be used to calculate the parameters for  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ , and  $S_{22}$ . By placing these parameters in a file and using them in Libra as a "Linear Data File Element," a simulation of the circuit can be

performed. A single stub matching network can be calculated for each circuit at 2.4 and 2.6 GHz. A simulation for the two detector circuits is shown in Figure 12. By using a larger impedance (100 ohm) line between the load and the stub (50 ohms), more predictable results can be obtained in the transition from simulation to the testing of the actual circuit. After the design has been simulated and tuned, the schematic can then be synchronized, exported, and milled. A tutorial for designing a detector circuit has been written and is currently located on Dr. Furse's web site in the tutorials section. The layout of one of the detector circuits is shown in Figure 13.

The circuit is tested using the network analyzer as explained previously. The important parameter to measure is  $S_{11}$ . Its value should be on the order of  $-20$  dB. Copper tape can be used to fine tune the circuit if necessary.

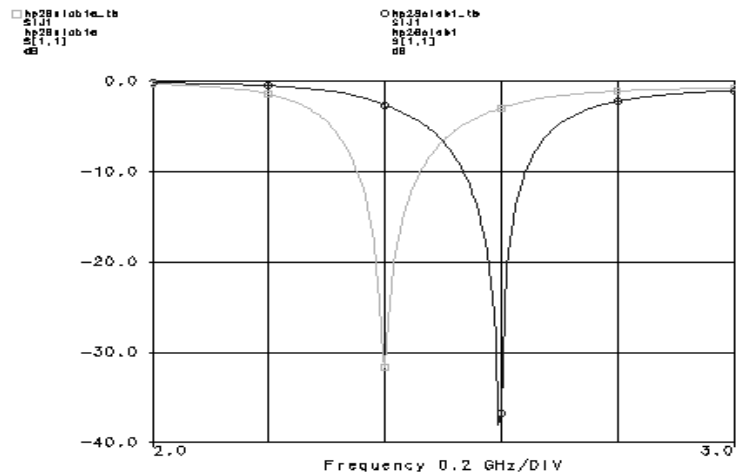


Figure 12. Detector Simulations

Another way to test the circuit is by using the signal source and a digital voltmeter. When the proper frequency is placed on the input of the circuit, a DC voltage should appear on the output after the diode. With an input power of 0 dBm, an output voltage of at least 1 V is expected for both detectors.



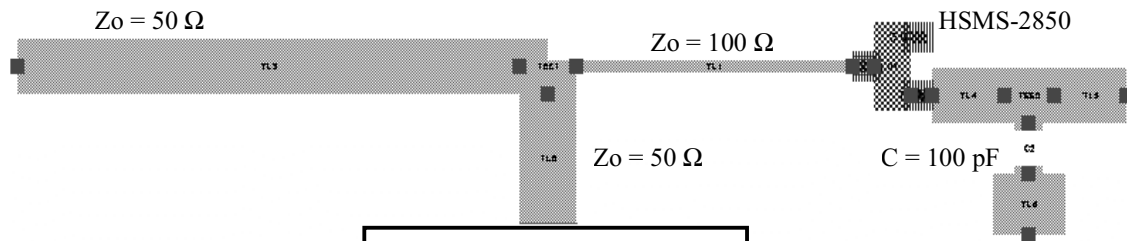


Figure 13. Detector Layout

## A/D Converter

The A/D converter is similar to the transmitter circuit. The outputs of each detector circuit are connected to the input terminals of a comparator (LM 311). The rail voltages are set to +12 V and -12 V. The output of the comparator is connected to the receive pin (pin 2) of a DB-9 serial cable. The grounds from the signal source and the chassis ground (pin 5) are connected together. The circuit will effectively produce a 1 or 0 depending on whether a frequency of 2.4 GHz or 2.6 GHz is received and detected in the circuit. Once again the program for serial communications is used to receive the data that is detected by the circuit.

The receiver circuit has been tested by taping the amplifier, power splitter, filters, and detectors together using copper tape and scotch tape. The transmitter is then connected to the front end of the amplifier in the receiver circuit using a coaxial cable. The serial communications software operates on both the transmitting and receiving computers and proper functionality of the circuit can be verified. Correct values at the receiver can be obtained with a transmitted power as low as -9 dBm. The highest speed for the local area network to work at is 9600 baud when the transmitter is connected directly to the receiver using a coaxial cable. Faster speeds produce different characters than those that are transmitted. When the antennas are attached, the performance decreases greatly. The maximum transmission rate with the antennas is 50 baud.

## Future Improvements

This project has many possibilities for improvements that can be performed. The antennas used in the project function as designed, but a more directional set of antennas would be desirable. The design is modular enough that antennas can be exchanged easily and tested with the circuitry. Another upgrade is to add an additional amplifier to the circuit. With more gain, the range of the wireless local area network can be improved. Another modification is to use an amplifier between the transmitter and the transmitting antenna to add more power and increase the range of the circuit. The most consequential modification would be to design a transmitter circuit using a voltage-controlled oscillator, an amplifier, and an antenna. With an operational transmitter, the circuit would be complete and then the task of trying to make a bi-directional link could be attempted. The current state of the circuit allows new parts to replace old parts with very little trouble. The possibilities for improvements are virtually limitless.

## Conclusion

The experience of designing, simulating, building, and testing high frequency circuits has been invaluable. Through the process of this project, practical knowledge has been gained about realistic projects in industry. The internet, data books, and suggestions from practicing engineers have all provided insights about general and specific topics in Electrical Engineering. After having such a positive experience, the future seems promising and bright.